REMARKS

Claims 1, 3, 5, 7, 8, 10, 12, 14 and 22-26 are pending in the present application. Claims 1 and 8 have been amended. Claims 22-26 have been presented herewith. Claims 6 and 13 have been canceled.

Claim Rejections – 35 U.S.C. 102

Claims 1, 3, 5, 6, 8, 10, 12, 13, 15, 17, 19 and 20 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Brunolli et al. reference (U.S. Patent No. 6,201,491). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

Claim 1 has been amended to include the features of dependent claim 6, and thus further features that "the first potential is a reference potential and the second potential is a ground potential". Applicant respectfully submits that the digital-to-analog converting circuit of claim 1 distinguishes over the Brunolli et al. reference as relied upon for at least the following reasons.

The Examiner has interpreted switches S_9 through S_{12} in Fig. 3 of the Brunolli et al. reference as the first switching circuit of claim 1, and switches S_1 through S_4 as the second switching circuit of claim 1.

As emphasized on page 8 of the Amendment dated July 31, 2006, column 3, lines 3-6 of the Brunolli et al. reference describes that the digital potentiometer may be fabricated on an integrated circuit die using complimentary metal oxide semiconductor

(CMOS) transistors for the switches. In other words, this would mean that switch S_{11} in Fig. 3 of the Brunolli et al. reference for example, would include a pair of coupled PMOS and NMOS transistors connected at one end to Vcc and connected at the other end to the node between resistors R_{LSB}. Each of switches S_1 through S_{12} would be configured in a somewhat similar manner.

As further emphasized in the above noted Amendment dated July 31, 2006, since each of switches S_9 through S_{12} in Fig. 3 of the Brunolli et al. reference are CMOS switches that include both PMOS and NMOS transistors, switches S_9 through S_{12} cannot be interpreted as the first switching circuit of claim 1, which is featured as "including P-channel type MOS transistors, each of the P-channel type MOS transistors connected directly to the first potential terminal, and to respective ones of the first connecting points and the first node, wherein only the P-channel type MOS transistors are connected to the first resistors as switches". For somewhat similar reasons, switches S_1 through S_4 in Fig. 3 of the Brunolli et al. reference cannot be interpreted as the second switching circuit of claim 1.

In view of these arguments as presented in the Amendment dated July 31, 2006, the Examiner has noted in the Response to Amendments/Arguments beginning on page 2 of the Final Office Action dated September 20, 2006, that the Brunolli et al. reference discloses in column 4, lines 45-51 "N-channel and P-channel metal oxide semiconductor (NMOS and PMOS), complementary metal oxide semiconductor (CMOS), bipolar transistor, junction field effect transistor (JFET), insulated gate field

effect transistor (IGFET) and the like, may be used to implement the switches and other circuits according to the embodiments of the present invention". The Examiner has asserted that an artisan in the art would thus have a choice of using N-channel and P-channel transistors as switches "***the same way 'complementary metal oxide (CMOS) transistors for the switches' may be used***", and that the argument as presented in the Amendment dated July 31, 2006 is therefore moot. Applicant respectfully disagrees for the following reasons.

As noted above, the Examiner has suggested that an artisan would have a choice of using N-channel and P-channel transistors as switches the same way the complementary metal oxide (CMOS) transistors are used for the switches in the Brunolli et al. reference. However, if N-channel transistors were used the same way as CMOS transistors in Fig. 3 of the Brunolli et al. reference, **all of switches S_1 through S_{12} would be N-channel transistors**, and the Brunolli et al. reference would not include a first switching circuit including P-channel type MOS transistors, as would be necessary to meet the features of claim 1. In a similar manner, if P-channel transistors were used the same way as CMOS transistors in Fig. 3 of the Brunolli et al. reference, **all of switches S_1 through S_{12} would be P-channel transistors**, and the Brunolli et al. reference would not include a second switching circuit including N-channel type MOS transistors, as would be necessary to meet the features of claim 1.

Applicant respectfully submits that the Brunolli et al. reference does not disclose or even remotely suggest using a specific first type of switch in a first switching circuit,

and using a different specific second type of switch in a second switching circuit, as would be necessary to meet the features of claim 1. In absence of such a clear teaching or suggestion in the Brunolli et al. reference, the Examiner has clearly relied upon impermissible hindsight to maintain this rejection. **If this rejection is to be maintained, the Examiner is respectfully requested to identify the specific motivation in the Brunolli et al. reference as relied upon that would suggest using respectively different types of switches in a corresponding converting circuit.**

As also noted above, claim 1 has been amended to feature that the first potential is a reference potential and the second potential is a ground potential. Applicant notes that a threshold voltage of an N-channel type MOS transistor has positive voltage level (for example + 0.7v). Thus, if switches S_9 and S_{12} in Fig. 3 of the Brunolli et al. reference were N-channel MOS transistors, each of output voltages from switches S_9 - S_{12} would become a voltage that falls down below supply voltage Vcc by the threshold voltage. Thus, the voltage applied at one end of each of the string of resistors (the end connected to the switch) is a voltage that falls down below the supply voltage Vcc by the threshold voltage.

In the digital-to-analog converting circuit of claim 1, the first switching circuit includes P-channel MOS transistors. P-channel MOS transistors are capable of transmitting a supply voltage at a source electrode to a drain electrode substantially without a drop in voltage during an ON state, when the P-channel MOS transistor is connected to a supply voltage potential side (first potential). Each of the output

voltages from each transistor of the first switching circuit therefore becomes a voltage substantially the same as the first potential level. Thus, by use of the first switching circuit of claim 1 including only P-channel type MOS transistors connected to the first resistors as switches, negative impact as resulting from different threshold voltage levels of the transistors can be prevented.

In a somewhat similar manner, the use of only N-channel type MOS transistors as switches connected to the second resistors in the second switching circuit of claim 1 prevents negative impact resulting from different threshold voltage levels of the transistors. Since the Brunolli et al. reference does not disclose or even remotely suggest using specific different types of switches in different switching circuits, the Brunolli et al. reference clearly does not recognize the above noted concepts, and consequently does not disclose or even remotely suggest the features of claim 1. Applicant therefore respectfully submits that the digital-to-analog converting circuit of claim 1 distinguishes over the Brunolli et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1, 3 and 5, is improper for at least these reasons.

The digital-to-analog converting circuit of claim 8 has been amended to include the features of dependent claim 13, and thus features that "the first potential is a reference potential and the second potential is a ground potential". Applicant respectfully submits that the digital-to-analog converting circuit of claim 8 distinguishes over the Brunolli et al. reference as relied upon for at least somewhat similar reasons

as claim 1. The Brunolli et al. reference does not suggest using a specific first type of switch connected directly to a first potential terminal, and a different specific second type of switch connected to a second potential terminal. The Brunolli et al. reference also fails to recognize and prevent negative impact of different threshold voltage levels of transistors. Applicant therefore respectfully submits that the digital-to-analog converting circuit of claim 8 distinguishes over the Brunolli et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 8, 10 and 12, is improper for at least these reasons.

Claim Rejections – 35 U.S.C. 103

Claims 7, 14 and 21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Brunolli et al. reference in view of the Leung et al. reference (U.S. Patent No. 6,400,300). Applicant respectfully submits that the Leung et al. reference as secondarily relied upon does not overcome the above noted deficiencies of the primarily relied upon Brunolli et al. reference. Accordingly, Applicant therefore respectfully submits that claims 7 and 14 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection is improper for at least these reasons.

Claims 22-26

The digital-to-analog converting circuit of claim 22 includes in combination

among other features a control circuit "connected to the first and second switching circuits for selectively turning on only one of the P-channel type MOS transistors and one of the N-channel type MOS transistors at a time, to provide the analog signal at the output node".

As may be readily understood in view of Fig. 4 of the Brunolli et al. reference, each state of the potentiometer illustrated in Fig. 3 includes three activated switches. The Brunolli et al. reference as relied upon thus clearly does not disclose a circuit in which only one of a P-channel type MOS transistor and one of an N-channel type MOS transistor are selectively turned on at time to provide an analog signal at an output node, as would be necessary to meet the features of claim 22. Applicant therefore respectfully submits that claims 22-26 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least these reasons.

Conclusion

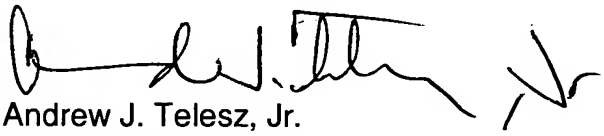
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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